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RECENT DEVELOPMENTS IN PARAMETRIC MULTIPLIERS

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ABSTRACT

Continuing work on parametric multiplier theory at M.I.T. has resulted in several interesting developments. The idler theory has been augmented to include the 1-2-3-4 quadrupler and the 1-2-4-6-8 octupler. The results thus far indicate that "extra" idlers can significantly improve both efficiency and power handling over the minimal idler case. The overdriven doublers, both abrupt and graded have been analyzed with simple models for the forward characteristics. As expected, power handling increases greatly, accompanied by a significant increase in efficiency. The most efficient doubler uses an overdriven graded junction. Experimental results are described together with observations on the causes and cures of spurious oscillations.

AUTHOR

I. INTRODUCTION

This paper is a compendium of some of the theoretical and experimental work carried out at M.I.T. and Lincoln Laboratory since the summer of 1962 on varactor multipliers. Diamond (Ref. 1 and 2) has carried out analyses on the effects of "extra" (larger number than necessary) idlers on quadruplers and octuplers with somewhat surprising results. An analysis has also been made on overdriven doublers using both abrupt- and graded-junction diodes (Ref. 3) with very simple models assumed for the forward characteristics. The results of the overdriven doublers lead to simple analysis techniques for doublers using diodes with radical nonlinear capacitance. Some experimental circuits have been developed which yield stable, high-efficiency, low spurious-content operation.

The use of more idlers than necessary yields higher efficiency and power handling than does the use of just the necessary number. When overdriven, the graded junction shows higher efficiency than the abrupt-junction in the doubler circuit. Care in circuit design can result in stable, clean operation of frequency multipliers.

II. EXTRA IDLE[illegible]

As is now well-known, non-overdriven abrupt-junction multipliers of order greater than X2 require currents flowing at some of the lower harmonics in order that non-zero output be achieved. The necessary "idler" frequencies can easily be identified by realizing that the junction voltage is proportional to the square of the junction charge. As shown in Penfield and Rafuse (Ref. [illegible]), the necessary idler configurations for some of the low-order multipliers become

(a) Tripler: 1-2-3
(b) Quadrupler: 1-2-4
[illegible]
(d) Sextupler: 1-2-3-6, 1-2-[illegible]
(e) Septupler: 1-2-3-6-7, 1-2-[illegible]-7,
1-2-3-5-7, 1-2-3-4-7, 1-2-[illegible] 8-7*
(f) Octupler: 1-2-4-8

Note that these idler schemes contain the minimum necessary number of idlers. The septupler marked with the asterisk is unusual in that an idler at a frequency higher than the output frequency is necessary for output at

The question that now arises concerns the effect of "unnecessary" or "extra" idlers.

[redacted]

For example, although the 1-2-4 quadrupler configuration will operate efficiently, what would be the effect of adding an extra idler to form a 1-2-3-4 quadrupler? Similarly, what would be the effects produced in a 1-2-3-4-5 quintupler or a 1-2-4-6-8-octupler?

The problem is very complex and can, in general, only be solved by detail computation, with the aid of a digital computer, on each multiplier. Two solutions for extra-idler multipliers have been obtained by Diamond (Ref. 1 and 2), namely, the 1-2-3-4 and 1-2-4-6-8. The results are of extreme interest.

PARAMETER	1 - 2 - 4	1 - 2 - 3 - 4
EFFICIENCY $\epsilon \simeq e^{-\alpha(\omega_{out}/\omega_c)}$	$\alpha = 15.6$	$\alpha = 11.4$
POWER INPUT $P_{in} \simeq \beta (V_B + \phi)^2 C_{min} \omega_o$	$\beta = 0.0196$	$\beta = 0.0226$
INPUT RESISTANCE $R_{in} \simeq A\, S_{max}/\omega_o$	$A = 0.150$	$A = 0.096$
LOAD RESISTANCE $R_4 \simeq B\, S_{max}/\omega_o$	$B = 0.0513$	$B = 0.0625$
BIAS VOLTAGE $\hat{V} = \dfrac{V_0 + \phi}{V_B + \phi}$	$\hat{V} = 0.334$	$\hat{V} = 0.330$

TABLE I. COMPARISON OF 1-2-4 AND 1-2-3-4 QUADRUPLERS. In each case, the idler circuit loss is assumed zero (only diode loss present). Values are useful for $\omega_{out} < 0.1\,\omega_c$.

First, we compare the two quadrupler configurations in the notation of Penfield and Rafuse (Ref. 4). The symbols used in the tables to follow are:

$\omega_c = S_{max}/R_s$ the varactor cutoff frequency (at breakdown)
ω_o = drive frequency
ω_{out} = output frequency
R_s = varactor series loss resistance
$C_{min} = S_{max}^{-1}$ = minimum junction capacitance (at V_B)
V_B = breakdown voltage
ϕ = contact potential
V_0 = average bias voltage

The others are self-explanatory. The formulation for low-frequency efficiency is due to Uhlir (Ref. 5).

We note in Table I that the 1-2-3-4 configuration has not only higher efficiency, but higher power handling (without overdriving) as well. Perhaps the lossless idler approximation masks some disabilities of the 1-2-3-4 quadrupler. If we assume an idler loss resistance equal in value to the varactor series loss resistance R_s (external idler circuit Q = diode Q) and again compare the two circuits $\alpha(1\text{-}2\text{-}4) = 25$ and $\alpha(1\text{-}2\text{-}3\text{-}4) = 16$, $\beta(1\text{-}2\text{-}4) = 0.020$ and $\beta(1\text{-}2\text{-}3\text{-}4) = 0.023$. It is obvious that the presence of idler loss only serves to accentuate the better efficiency of the 1-2-3-4 circuit over the 1-2-4. The power levels are relatively unchanged.

[redacted]

PARAMETER	1 - 2 - 4 - 8	1 - 2 - 4 - 6 - 8
EFFICIENCY $\epsilon \simeq e^{-\alpha(\omega_{out}/\omega_c)}$	$\alpha = 21.0$	$\alpha = 14.9$
POWER INPUT $P_{in} \simeq \beta (V_B + \phi)^2 C_{min} \omega_o$	$\beta = 0.0198$	$\beta = 0.0248$
INPUT RESISTANCE $R_{in} \simeq A\, S_{max}/\omega_o$	$A = 0.103$	$A = 0.140$
LOAD RESISTANCE $R_8 \simeq B\, S_{max}/\omega_o$	$B = 0.0188$	$B = 0.0251$
BIAS VOLTAGE $\hat{V} = \dfrac{V_o + \phi}{V_B + \phi}$	$\hat{V} = 0.351$	$\hat{V} = 0.347$

TABLE II. COMPARISON OF 1-2-4-8- AND 1-2-4-6-8 OCTUPLERS. In each case idler circuit loss is zero. Values are good for $\omega_{out} < 0.1\,\omega_c$.

A similar comparison is made between the 1-2-4-8 and 1-2-4-6-8 octuplers in Table II. It is again obvious that the 1-2-4-6-8 configuration exceeds in both efficiency and power handling the 1-2-4-8 octupler. As before, a comparison with equal external idler and diode Q's gives α(1-2-4-8) = 31.3 and α(1-2-4-6-8) = 23.1, β(1-2-4-8) = 0.020 and β(1-2-4-6-8) = 0.025. It is apparent that the extra idler gives improved performance even with idler loss included.

One is tempted to make some fairly general conclusions from the admittedly sparse data obtained so far. Table III presents the α and β for a group of varactor multipliers. If we extrapolate the results for the quadrupler to the quintupler and sextupler it appears that the addition of the $3\omega_o$ idler to give a 1-2-3-4-5 quintupler and the $3\omega_o$ and $5\omega_o$ idlers to give a 1-2-3-4-5-6 sextupler would result in α's and β's commensurate with the X2, X3 and X4 (1-2-3-4) circuits. It is also very tempting to estimate that the addition of extra

[illegible]	α	β
X2*	[illegible].95	0.0[illegible]
X3*	11.6	0.0241
X4(1, 2, 3, 4)	11.[illegible]	0.0226
X5(1, 2, 4, 5)*	18.6	0.018
X6(1, 2, 4, 6)*	16.6	0.022
X8(1, 2, 4, 6, 8)	14.9	0.0248

TABLE III. α AND β FOR VARIOUS MULTIPLIERS.* Data taken from Penfield and Rafuse (Ref. 4).

idlers to the octupler to yield a 1-2-3-4-5-6-7-8 octupler would bring the octupler results into line with the rest of the multipliers. However, the computational complexity required to check such results is extremely high. It is hoped that future work may lead to a unified theory which will predict essentially equivalent efficiencies (in terms of the output frequency to cutoff frequency ratio) and equivalent power handling capabilities (in terms of the input frequency) for the same diode, regardless of the order of multiplication. In this vein it is interesting to note that the 1-2-4-6-8 octupler is already more efficient than the 1-2-4 quadrupler (for the same output frequency).

III. OVERDRIVEN DOUBLERS

An analysis has been carried out at M.I.T. on the overdriven abrupt- and graded-junction doublers (Ref. 6). The model chosen for the forward region was exceedingly simple; it was assumed that the diode elastance (C^{-1}) went to zero at charges greater than the charge equivalent to the contact potential, and it was further assumed that the series resistance remained constant in the forward direction. Both of these assumptions, although radical, are fair approximations. The series-loss resistance will, of course, be reduced by conductivity modulation effects in the forward direction, but a good part of the losses in high-quality varactors occurs in the contacts and leads and

PARAMETER	MODE	ABRUPT-JUNCTION	GRADED-JUNCTION
EFFICIENCY $\epsilon \simeq e^{-\alpha(\omega_{out}/\omega_c)}$	OVERDRIVEN	$\alpha = 7.5$	$\alpha = 7.0$
	NOMINAL	$\alpha = 9.95$	$\alpha = 12.8$
POWER INPUT $P_{in} \simeq \beta (V_B + \phi)^2 C_{min} \omega_o$	OVERDRIVEN	$\beta = 0.0680$	$\beta = 0.0680$
	NOMINAL	$\beta = 0.0277$	$\beta = 0.0118$
INPUT RESISTANCE $R_{in} = A\, S_{max}/\omega_o$	OVERDRIVEN	$A = 0.100$	$A = 0.110$
	[illegible]	$A = 0.080$	$A = 0.0604$
LOAD RESISTANCE $R_2 = B\, S_{max}/\omega_o$	OVERDRIVEN	$B = 0.164$	$B = 0.170$
	NOMINAL	$B = 0.136$	$B = 0.102$
BIAS VOLTAGE $\hat{V} = \dfrac{V_0 + \phi}{V_B + \phi}$	OVERDRIVEN	$\hat{V} = 0.258$	$\hat{V} = 0.258$
	NOMINAL	$\hat{V} = 0.349$	$\hat{V} = 0.409$
EFFECTIVE INPUT ELASTANCE $\hat{S}' = S_{in}/S_{max}$	OVERDRIVEN	$\hat{S}' = 0.33$	$\hat{S}' = 0.37$
	NOMINAL	$\hat{S}' = 0.50$	$\hat{S}' = 0.68$
EFFECTIVE OUTPUT ELASTANCE $\hat{S}'' = S_{out}/S_{max}$	OVERDRIVEN	$\hat{S}'' = 0.36$	$\hat{S}'' = 0.40$
	NOMINAL	$\hat{S}'' = 0.50$	$\hat{S}'' = 0.67$

TABLE IV. COMPARISON OF OVERDRIVEN AND NON-OVERDRIVEN ABRUPT- AND GRADED-JUNCTION DOUBLERS. Results valid for $\omega_{out} < 0.1\,\omega_c$.

therefore the total loss will remain essentially constant. The elastance does not actually go to zero but instead simply decreases exponentially (along with an increasing conductance, yielding a very low junction Q) ; however, at the frequencies of interest the junction impedance level is so low that the diode can be reasonably represented by just the series loss, R_s.

The results for optimum efficiency operation of the optimally overdriven graded- and abrupt-junction doublers are given in Table IV along with the results for nominal drive (see Ref. 4) for comparison. The most startling result (although one rather frequently and often embarrassingly observed experimentally) is that the two types of diodes, optimally overdriven, give essentially equal performances. For the same power input, same breakdown voltage and same minimum capacitance , the graded-junction and abrupt-junction diodes are essentially interchangeable in any doubler circuit. The bias voltages are identical, the input and output resistances and reactances are essentially the same, and the efficiencies are practically equal.

It is interesting to note that the graded junction diode must be overdriven by a factor of 5.8 (in power) , whereas the abrupt-junction diode optimizes when overdriven by only a factor of 2.45. Furthermore , the graded junction shows the most improvement in efficiency and actually exceeds the efficiency of an abrupt junction when optimally overdriven.

A second important result which wa[illegible] not obvious (at least to the author) before the computer derivation of the overdriven doubler was completed, lies in the ratio of fundamental to second-harmonic charge. If the power output is optimized, the low-frequency value of the ratio is 2.0, regardless of the diode type or the level of overdriving. One suspects that this result holds true almost universally.

If we assume such a universal behavior, we can calculate the performance for a variety of other diode types. In particular , we can postulate the "ideal" diode characteristic shown in Fig. 1 and overdrive so that the elastance waveform is a square-wave of peak-to-peak value S_{max}. Such a curve is actually approximated by some of the very thin diffused, epitaxial diodes, where the majority of the elastance change takes place over the first few volts in the back direction and practically no change in elastance occurs for higher voltages, until breakdown is reached.

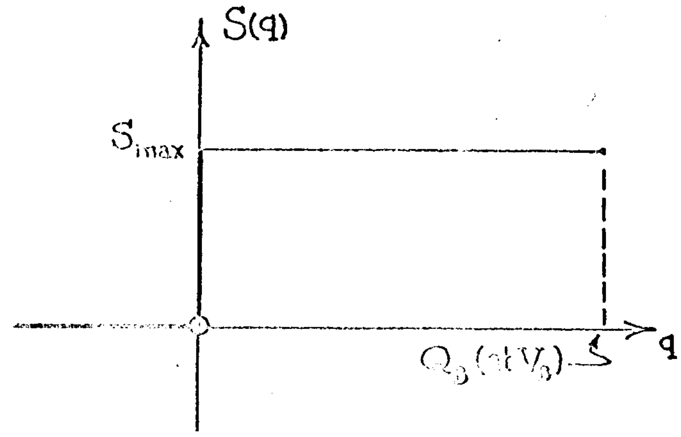

FIG. 1. STEPWISE NONLINEAR ELASTANCE CHARACTERISTIC.

If we assume a constant series resistance R_s, we can calculate efficiency, power, input and output resistances and the rest of the necessary parameters with ease.

In Appendix A a detailed derivation of the overdriven stepwise-diode doubler is presented. It should be noted that such a device will <u>not</u> multiply unless it is overdriven, otherwise it appears as a constant elastance. The results are interesting . Presented in Table V are the efficiency, input power and input and load resistances for such an overdriven doubler, together with the same parameters for the overdriven abrupt- and graded-junction doublers operating under the same conditions (optimum power output, fully driven, average charge equal to zero).

[illegible] increases as the diode becomes, if you wish, more and more nonlinear. Although, the power-handling capability decreases. In other words, one trades efficiency for power handling. Although the stepwise doubler probably does not have the best achievable efficiency (allowing higher harmonic currents to flow may give better efficiency) , it is useful in predicting the behavior of overdriven epitaxial units.

IV. SOME OBSERVATIONS ON γ = 0.45 AND SO FORTH . . .

Many people still insist on characterizing a varactor as "not quite abrupt" or "not quite graded" with, therefore, exponents that lie between 1/2 and 1/3. The author has never seen one of these "not quite" varactors.

Every diode has associated with it certain parasitic elements. At low frequencies, where most varactor capacitance measure-

PARAMETER	STEPWISE	GRADED	ABRUPT
EFFICIENCY	$\alpha = 4.7$	$\alpha = 8.25$	$\alpha = 10.5$
INPUT POWER	$\beta = 0.063$	$\beta = 0.091$	$\beta = 0.115$
INPUT RESISTANCE	A = 0.212	A = 0.121	A = 0.095
LOAD RESISTANCE	B = 0.212	B = 0.121	B = 0.095

TABLE V. COMPARISON OF EFFICIENCY, INPUT POWER AND INPUT AND LOAD RESISTANCES FOR OVERDRIVEN STEPWISE -, GRADED - AND ABRUPT-JUNCTION DOUBLERS. In each case the diode is driven to the breakdown voltage, output power is optimized and the average charge is zero. The symbols α, β, A and B correspond to those in Table IV.

ments are made, the major parasitic is case capacitance. The total capacitance can therefore be written as

$$C = C_{case} + C_{min}\left[\frac{V_B + \phi}{v + \phi}\right]^{\gamma} \quad (1)$$

where $\gamma = 1/2$ for abrupt junctions and 1/3 for graded. Extremely careful measurements were made on several abrupt- and graded-junction varactors with a three-terminal capacitance bridge (Boonton 75A-S8) and a digital voltmeter.

In no case was a diode found to have an exponent other than 0.500 or 0.333. If careful measurements are made and V_B determined accurately, three points suffice to determine the three unknowns, ϕ, C_{case} and C_{min}. For example, careful measurements on a PSI PC-115-10 diode yielded V_B = 114.0 volts, ϕ = 0.540 volts, C_{min} = 1.81 pf and C_{case} = 0.937 pf. A plot of $(C - C_{case})^{-2}$ versus v yielded an absolutely straight line with 17 data points lying on the line. The exponent was precisely 0.500.

Other measurements made on epitaxial units yielded straight lines for $(C - C_{case})^{-3}$ versus v, but the values of C_{min}, V_B and would change abruptly at some voltage less than breakdown. The characteristic S^3 versus v was composed of two straight segments, one from ϕ to V_a ($< V_B$) and one of lesser slope from V_a to V_B. In many units with V_B in the order of 50 volts, the break voltage V_a was only 6-8 volts. The practice of giving the cutoff frequency of such units at 2, 4 or 6 volts in the reverse direction (depending on the particular manufacturer's crystal ball) can give large errors in extrapolated C_{min} and f_c at breakdown. The errors are unfortunately in the optimistic direction and the units will not perform as expected. If C_{min} and f_c at V_B were given, the units would be far more conservatively characterized and multiplier performance would be more easily predicted.

In short, if the diode is characterizable by an exponent <u>over its entire voltage range</u> (which rules out the so-called "hyper-abrupt" units) the exponent is either 1/2 or 1/3, not 0.45, 0.36 or some other approximation, arrived at by neglecting the case capacitance or not recognizing the break in the epitaxial units.

V. CIRCUIT TECHNIQUES

In this section are described some circuit techniques found useful at M.I.T. Unfortunately, at this time good experimental data on overdriven doublers is not available. However, a very detailed design of a symmetric, two-diode tripler was carried out with quite satisfying results.

The tripler was built with two nearly matched PSI PC-117-47 varactors (with measured characteristics of C_{min} = 6.6 and 6.9 pf, $V_B + \phi$ = 138 v. (lowest one of the

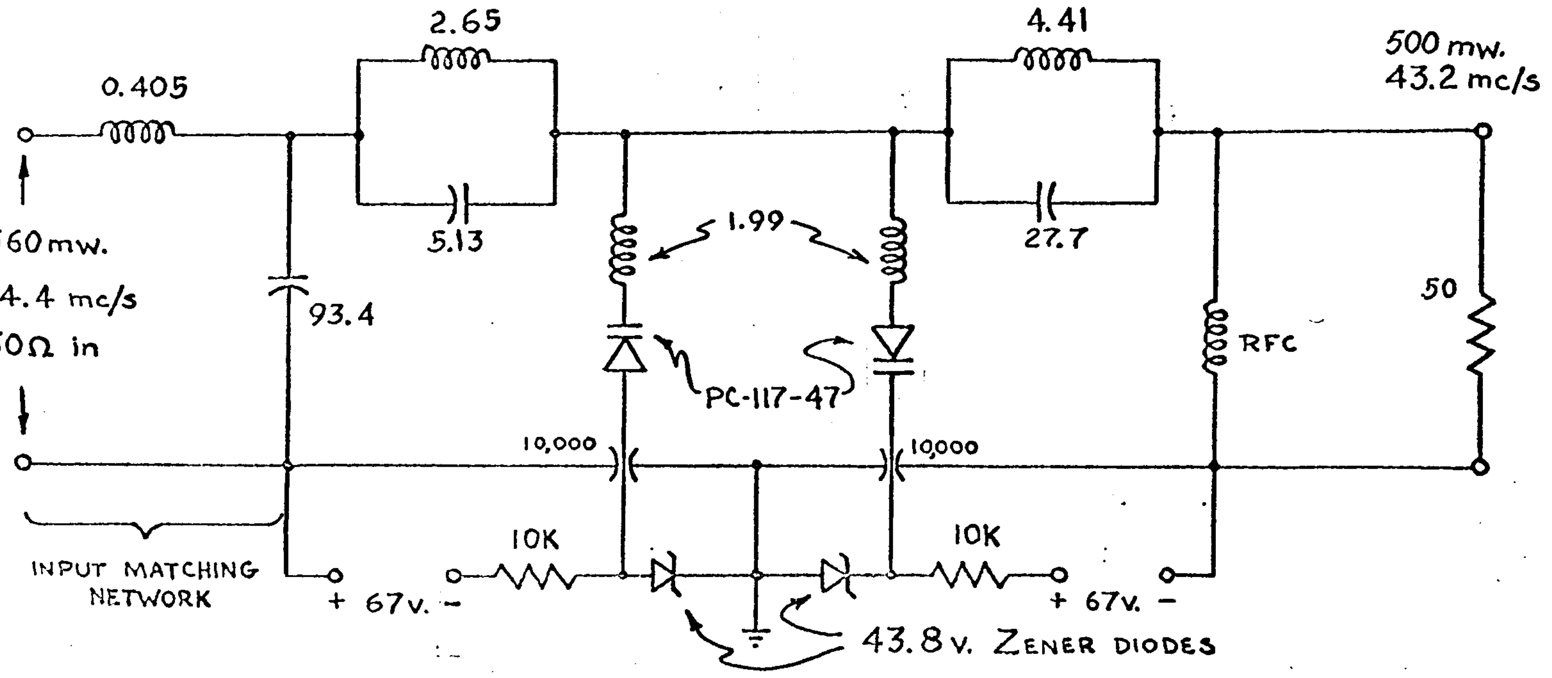

FIG. 2. TRIPLER CIRCUIT. Values of the components are in pf, μh and ohms.

pair), ϕ = 0.64v., C_{case} = 2.3 and 1.4 pf). Both the case capacitances and the strays were used in determining the input matching network necessary to give a match to 50Ω source at the design power level. The idler at $2\omega_o$ is resonated in the loop formed by the two varactors and the two 1.99 μh coils. Two parallel-resonant traps separate the currents at ω_o and $3\omega_o$ into the input and output circuits, respectively.

The losses in the individual circuits were measured and included in the efficiency calculations. The final operating conditions are compared with the predicted [illegible] Table VI. The agreement is embarrassingly

PARAMETER	THEOR.	EXPER.
CIRCUIT EFFICIENCY	90%	89.6%
LOAD RESISTANCE	50Ω	50Ω
INPUT RESISTANCE	50Ω	48.5Ω
POWER INPUT	560 mw.	558 mw.
BIAS VOLTAGE	43.7 v.	43.8 v.

TABLE VI. THEORETICAL AND EXPERIMENTAL PARAMETERS FOR THE SYMMETRIC TRIPLER.

close, in fact, closer than the accuracy of the measuring instruments. However, it shows that one can design with care and achieve very close agreement with theory.

Several other interesting observations can be made. First, the multiplier would not operate self-biased (not very much effort was spent trying) and would simply break up into spurious oscillations before any appreciable output power could be reached. Second, biased at the proper voltages from potentiometers, the tripler was stable, until the frequency was [illegible] to overdrive; in either case it broke up into spurious oscillations. Third, the majority of the spurious oscillations were identified at their baseband frequency (500-1000 kc/s) in the bias circuitry; the addition of the Zener diodes to the bias circuit provided a sufficiently low enough incremental impedance to swamp the spurious generation mechanism. Under these conditions the 1 db bandwidth of the tripler became 7% and it could be overdriven up to a factor of 1.5 (limited by the driving source) with no sign of spurious oscillations. In fact, it was very difficult to establish any sort of spurious oscillation; only a radical (20-30%) change in input frequency would excite a divide-by-two or divide-by-three mode. Fourth, a 1-2-4-5 quintupler was built as a following stage; it was noted that the output at 216 mc/s was spurious free only if the input of the quintupler was tuned properly and presented a

50Ω load to the tripler. It appears that many of the problems arising during the cascading of multipliers can be cured with careful design of each individual stage.

A spectrum analyzer was used to check the level of the fundamental and unwanted harmonics at the tripler output. The fundamental and all even harmonics were down 40 db. The fifth harmonic was most prevalent, but still 30 db down. Additional filtering could easily be added to reduce the unwanted signals to 80 db below the output, if desired.

VI. CONCLUSIONS

Perhaps the major conclusion one comes to is that there remains a considerable amount of work to be done before parametric multipliers can be considered "fully understood." "Conclusion jumping" in the field of parametric multipliers is a technique fraught with danger. The author remembers when he considered extra idlers equal to extra loss. Unfortunately, intuition seems to work only in a posteriori sense for parametric multipliers.

However, disregarding the dangers of intuitive reasoning, it appears from the results of the 1-2-3-4 and 1-2-4-6-8 multipliers that extra idlers can improve both the efficiency and power handling of a varactor multiplier, by non-trivial factors. It further appears (and this is even further out on the limb) that appropriate idler schemes will yield multipliers with nearly equal efficiencies (for the same diode and the same output frequency) and nearly equal power handling (for the same diode and the same input frequency).

Two important results appear in the analysis of the overdriven doublers. The overdriven graded-junction doubler is somewhat more efficient than the overdriven abrupt-junction doubler (precisely the opposite result one finds when nominally driving). For identical breakdown voltages and identical minimum capacitances, at the optimal overdrive level the abrupt-junction and graded-junction diodes are indistinguishable in a doubler.

A companion result from the overdriven analysis is the charge ratio of 2.0, when the output power is optimized. At low frequencies the ratio holds regardless of the degree of non-linearity. This allows us to compute the characteristics of an infinite variety of doublers and compare their performances.

A particular limiting case, the stepwise doubler, is analyzed and found more efficient than the graded junction, although of somewhat less power-handling capability. It appears that, as the degree of "non-linearness" of the varactor characteristic increases, the efficiency, when overdriven, increases and the power handling decreases.

Very careful measurements show that a diode can be characterized by an exponent over its full voltage range, only if the exponent is 1/3 or 1/2. Values of γ ranging between 0.500 and 0.333 are invariably the result of poor measurement procedure or improper subtraction of parasitic case capacitance. Some epitaxial units may show breaks in the elastance-voltage characteristic, but their exponents do not usually vary. If the diode exponent truly varies with back voltage, it cannot properly be said to have an exponent (even on the "average," whatever that means). Epitaxial units should be characterized by cutoff frequency and capacitance at breakdown, not some intermediate voltage.

Experimentally it has been observed that careful design will yield multiplier performance essentially as theory predicts. Spurious oscillations can be minimized if the bias-circuit impedance can be kept real and small at frequencies from low audio to an appreciable fraction of the drive frequency. A high-quality Zener diode makes an almost ideal bias source. Oscillations arising during cascading of multipliers can be minimized by insuring that the input impedance of the second multiplier is real and equal to the optimum load resistance for the first multiplier (this is, of course, achievable with an isolator; but such devices, besides being bulky and heavy, just do not exist below 100-200 mc/s.

Appendix A

DERIVATION OF STEPWISE-JUNCTION DOUBLER

If $S(q)$ is S_{max} for $0 < q \leq Q_B$ and zero for $q < 0$ and we assume that the fundamental charge is twice the second-harmonic charge, then, with the junction driven such that that charge wave just reaches the breakdown charge Q_B and averages to zero, we have

$$q(t) = \frac{2}{3\sqrt{3}} Q_B \left(2\sin\omega_o t + \sin 2\omega_o t\right) \quad (?)$$

[illegible] the currents "in phase."

The current is

$$i(t) = \frac{4}{3\sqrt{3}} Q_B \omega_o \left(\cos\omega_o t + \cos 2\omega_o t\right) \tag{3}$$

assuming all higher-harmonic currents open-circuited. The resultant square-wave of elastance becomes

$$S(t) = \frac{S_{max}}{2}\left[1 + \sum_{k=1}^{\infty} \frac{4}{\pi}\,\frac{1-(-1)^k}{2}\sin k\omega_o t\right] \tag{4}$$

The equation of motion for the junction is

$$v(t) = \int S(t)\, i(t)\, dt \tag{5}$$

and, substituting Equations (3) and (4) in Equation (5) and integrating, we have the fundamental and second harmonic components of $v(t)$ as

$$v(t) = \text{[illegible]}\; S_{max} Q_B \left(\cos\omega_o t - \cos 2\omega_o t\right) \tag{6}$$

Now,

$$P_{in} = \frac{1}{2} I_1 V_1 = \frac{16}{81\pi} S_{max} Q_B^2 \omega_o \tag{7}$$

However, for the stepwise junction,

$$Q_B = V_B / S_{max} \tag{8}$$

so

$$P_{in} = 0.0628\, V_B^2 C_{min} \omega_o \tag{9}$$

where $C_{min} = S_{max}^{-1}$.

Now, we assume a series loss resistance, R_s, giving a cutoff frequency of

$$\omega_c = S_{max} / R_s \tag{10}$$

At low frequencies the dissipated power becomes

$$P_{diss} = \frac{1}{2}(I_1^2 + I_2^2) R_s = \frac{16}{27} Q_B^2 \omega_o^2 R_s \tag{11}$$

and the efficiency is

$$\epsilon \simeq 1 - \frac{P_{diss}}{P_{in}} = 1 - 3\pi \frac{\omega_o}{\omega_c} \tag{12}$$

We can write Equation (12) in the same form used for the other multipliers

$$\epsilon \simeq e^{-\frac{3\pi}{2}\left(\omega_{out}/\omega_c\right)} \tag{13}$$

Therefore, $\alpha = 4.7$ and $\beta = 0.0628$. The input and load resistances are equal and become

$$R_{in} = \frac{V_1}{I_1} = R_2 = \frac{V_2}{I_2} = \frac{2}{3\pi}\,\frac{S_{max}}{\omega_o} \tag{14}$$

or $A = B = 0.212$. The average elastance is the same at ω_o and $2\omega_o$; and is simply $S_{max}/2$.

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